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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/934,590	Applicant(s) HYONG-GON LEE	
	Examiner Abbas I Abdulselam	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/28/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 11-18* is/are rejected.

7)☒ Claim(s) *3,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Regarding claim 1, Applicant argues that Akiyama does not teach "a memory cell unit for receiving the first control signal and the second control signal from the control signal line". However, as shown in the art rejection below, Akiyama teaches storing means, a digital memory such as a semiconductor memory that stores digital data. Akiyama further teaches that when the data signal is a digital signal or when an analog data signal is converted into digital data by an analog-digital converter (ADC) or the like and stored, the digital memory can be used (col. 4, lines 32-37). Akiyama illustrates the use of a memory circuit (803) as part of structure of a pixel (Fig. 8) shown in a fourth embodiment, and it would have been obvious to one of ordinary skill in the art to utilize Akiyama's teaching of storing means as demonstrated in Fig. 8 in the structure of a pixel shown inside a second embodiment (Fig. 6) for the purpose of storing signals.

Regarding claim 5, Applicant argues that Akiyama does not teach "a level shift unit for receiving the second control signal, lifting the high rate state by as much as the second power, generating an inverting signal, and outputting the inverting signal. Akiyama teaches an inverting circuit (103) which includes a polarity inverter (105) as shown in Fig. 6. Akiyama also teaches the use of a comparator (15) with an output voltage of V2, (Fig. 1A) and wave shaper (4) of Fig. 1B. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Akiyama's inverting circuit (103) as configured in Fig. 6 along with the comparator (15) as configured in (Fig. 1A) and wave shaper (4) as configured in Fig. 1 for the

purpose of generating signals including different polarity, and manipulating power structure. Col. 15, lines 49-50 and Fig. 6.

Regarding claim 12, Applicant argues that Akiyama does not teach transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state. However, as shown in the art rejection below, Akiyama teaches data signal is supplied to the pixel (Fig. 9) which indicates still picture as input signals, discloses polarity inverter (105), indicates AC voltage applied to liquid crystal (col. 3, lines 23-24 DC, and is clear that Vr is an AC voltage as shown (Fig. 11C/D).

Regarding claim 16, applicant argues that Akiyama does not teach "a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage". However, as shown in the art rejection below, Akiyama discloses an inverting circuit (103) including a polarity inverter (105) in connection with flipflop (107) as shown in Fig. 6. Furthermore, Akiyama discloses that the output voltage V2 of an analog buffer 104 or an output voltage -V2 of the polarity inverter 105 are selected by the analog switches 106a and 106b and the selected voltage is supplied to the pixel electrode 114.

It would have been obvious to one of ordinary skill in the art to utilize the selection of voltage with respect to pixel electrode for the purpose of setting the amount of voltage needed.

Regarding claim 18, applicant argues that Akiyama does not teach "a source and scan driver being inactivated for a second period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the

second period". However, as shown in the art rejection below, Akiyama discloses an inverting circuit (103) including a polarity inverter (105) in connection with flipflop (107) as shown in Fig. 6. Akiyama further discloses that the output voltage V2 of an analog buffer 104 or an output voltage -V2 of the polarity inverter 105 are selected by the analog switches 106a and 106b and the selected voltage is supplied to the pixel electrode 114. Akiyama concludes that as shown in FIG. 6, an AC voltage is generated with an analog signal stored in the pixel unit. (Col. 15, lines 49-65 and Fig. 6 (107)). Akiyama teaches that when a still picture is displayed, after data signals for one screen are written to the storage capacitors (Cs2) 14 of all pixels, a relevant scanning line driving circuit is stopped; the relevant gate pulse (scanning signal) can be stopped; and the relevant signal line driver can be stopped. (Fig. 9 (902, 903) and col. 12, lines 26-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Akiyama's inverting circuit (103) as configured in Fig. 6 fro the purpose of inverting the polarity of a given signal in a desired fashion. It would have been obvious to utilize Akiyama's pixel electrode (114) as configured with analog switches (106a, 106b) along with Akiyama's teaching of relevant signals being stopped for the purpose of achieving inactivation with respect to drivers in a given period.

2. Applicant's arguments with respect to claims 16-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (US Patent 5,977,940).

As to claim 16, Akiyama et al. discloses a liquid crystal display (LCD), comprising a scan signal line (gate line 9, figure IA); a source signal line (signal line 8, figure l A); a pixel switch, a power unit for supplying a first power, a second power and a third power to pixels figure IA indicates each pixel comprises a comparator and waveform shaper 4, this implies power unit has to exist for supplying them power, also note column 12, power of driver circuits can be turned off, column 12, line 32) ; a first control signal line (Css line shown in figure 9) for transmitting a first control signal to the pixels; a second control signal line (Inversion signal line 112 shown in figure 6, column 16, lines 1314) for transmitting a second control signal to the pixels; and a level shift unit in electrical communication with the second control signal for generating an inverting signal (inverting circuit 103 with polarity inverter 105, column 15, lines 49-50 in electrical communication with inversion signal line via flipflop 107 shown in figure 6).

Akiyama does not teach "a level shift unit in electrical communication with the second control signal for generating an inverting signal and increasing a voltage". However, as shown in the art rejection below, Akiyama discloses an inverting circuit (103) including a polarity inverter (105) in connection with flipflop (107) as shown in Fig. 6. Furthermore, Akiyama discloses that the output voltage V2 of an analog buffer 104 or an output voltage -V2 of the polarity inverter 105 are selected by the analog switches 106a and 106b and the selected voltage is supplied to the pixel electrode 114.

It would have been obvious to one of ordinary skill in the art to utilize the selection of voltage with respect to pixel electrode for the purpose of setting the amount of voltage needed.

As to claim 17, a liquid crystal display of claim 16, wherein the level-shifting unit outputs the generated inverting signal (column 15, lines 60-62).

4. Applicant's arguments, see # 7, filed on 04/28/04, with respect to the rejection(s)of claim 18 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Akiyama (USPN 5977 940), same reference but rejected under 35 U.S.C. (103a).

As to claim 18, Akiyama et al. discloses a liquid crystal display, comprising: a scan driver (gate line driving circuit 903 in figure 9) activated to supply scanning signals for a first period and inactivated for a second period (relevant scanning line driving is stopped, column 12, lines 26-27); a source driver (signal line driving circuit 902 shown in figure 9) activated to

supply image signals for the first period and inactivated for the second period (relevant signal line driver is stopped, column 12, lines 28-29); and a plurality of pixels (column 17, lines 57-58), each pixel including a liquid crystal capacitor liquid crystal 5 shown in figure lA) displaying an image, a pixel switch (transistor 9 shown in figure IA) for transmitting the image signals in response to the scanning signal, and a memory cell storing and transmitting the image signal from the pixel switch to the liquid crystal capacitor (memory 202 shown in figure 7) during the first period and providing at least one of the stored image signal and an inversion signal to the stored image signal (polarity inverter 105, figure 6, column 15, lines 49-50) for the liquid crystal capacitor during the second period after data signals are written to the storage capacitors , column 12, lines 25-27).

However, Akiyama does not specifically teach "a source and scan driver being inactivated for a second period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the second period". However, as shown in the art rejection below, Akiyama discloses an inverting circuit (103) including a polarity inverter (105) in connection with flipflop (107) as shown in Fig. 6. Akiyama further discloses that the output voltage V2 of an analog buffer 104 or an output voltage -V2 of the polarity inverter 105 are selected by the analog switches 106a and 106b and the selected voltage is supplied to the pixel electrode 114. Akiyama concludes that as shown in FIG. 6, an AC voltage is generated with an analog signal stored in the pixel unit. (col. 15, lines 49-65 and Fig. 6 (107)). Akiyama teaches that when a still picture is displayed, after data signals for one screen are written to the storage capacitors (Cs2) 14 of all pixels, a relevant scanning line driving circuit is stopped; the relevant gate pulse (scanning signal) can be stopped; and the

relevant signal line driver can be stopped. (Fig. 9 (902, 903) and col. 12, lines 26-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Akiyama's inverting circuit (103) as configured in Fig. 6 fro the purpose of inverting the polarity of a given signal in a desired fashion. It would have been obvious to utilize Akiyama's pixel electrode (114) as configured with analog switches (106a, 106b) along with Akiyama's teaching of relevant signals being stopped fro the purpose of achieving inactivation with respect to drivers in a given period.

5. Applicant's arguments with respect to claims 1, 2, 4-8, 11-15 filed on 04/28/04 have been fully considered but they are not persuasive.

6. Claims 1, 2, 4-8, 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. (US Patent 5,977,940).

As to claim 1, Akiyama et al. discloses a liquid crystal display, comprising: a scan signal line (gate line 9 Gn shown in figure IA) for supplying scanning signals to pixels; a source signal line (signal line Sm 8 shown in figure l A) for supplying image pixels to a third electrode from a first electrode connected to the source signal line; a pixel switch (switch 801 shown in figure 8) for outputting the image signals to a third electrode; a power unit for respectively supplying first power and second power to all pixels (Note figure IA indicates that each pixel comprises a comparator and waveform shaper 4, this implies power unit has to exist for supplying them power, also note column 12, power of driver circuits can be turned off, column 12, line 32); a control signal line unit respectively including a first control signal line (Css line shown in figure

6) for transmitting a first control signal line to all pixels, and a second control signal line (Inversion signal line 112 shown in figure 6) for transmitting a second control signal to all pixels; a liquid crystal unit (liquid crystal layer 5, column 10, lines 29-30) for selectively transmitting according to voltage difference between the image signals and the second power; a memory cell unit (memory 803 shown in figure 8). However, Akiyama et al. fails to expressly teach memory cell unit for receiving the first control signal and the second control signal from the control signal line unit. Note Vref and Vcs are received by block 15 as shown in figure IA/B. It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Akiyama et al. then modify the control signal line unit to provide control of memory cell 803 to obtain the apparatus Akiyama et al. modified because it would accommodate driving of still image and moving image signals, and facilitate reduction of power of LCD driver.

As to claim 2, the liquid crystal display of claim 1, wherein said operation mode image signal data signal is supplied to the pixel, (column 9, lines 57-58), also is transmitted to the liquid crystal unit (liquid crystal 5, figure IA), when the first control signal is in low state and the second control signal is in high state, and when the first control signal is in high state. Akiyama et al. fails to expressly teach when the first control signal is in low state and the second control signal is in high state, and when the first control signal is in high state. Since Akiyama et al. teaches still picture and moving picture as shown in figure 9, switching transistor 802 controlling memory 803 shown in figure 8, it is obvious to one skilled in the art to vary control signals Vref and Vcs in order to drive the liquid crystal 5.

As to claim 4, the liquid crystal display (LCD) of claim 1, wherein the control signal line unit transmits control signals sequentially delayed by a buffer circuit to corresponding pixel

areas where the pixel area of the LCD panel is divided into at least two portions (buffer circuit has to exist in LCD driving circuit shown in figure 9 in order to remove noise, LCD panel 901 is divided into pixel arrays by signal lines 8 and gate lines 9, column 9, lines 47-54).

As to claim 5, Akiyama et al. discloses a low power liquid crystal display (LCD), comprising: a scan signal line (gate line 9, figure lA); a source signal line (signal line 8, figure lA); a pixel switch (transistor 1, figure l A) for selectively outputting image signals; a control signal line unit including a first control signal line (Css line 111 shown in figure 6, column 16, lines 33-34) and a second control signal line (Inversion signal line 112 shown in figure 6, column 16, lines 13-14); a liquid crystal unit (liquid crystal 5 shown in figure lA) for selectively transmitting according to a difference between the image signals (inversion of data signal to pixel electrode 114 shown in figure 6, column 15, lines 40-41) and the third power (Vcom shown in figure 6) a level shift unit for receiving the second control signal (inverting circuit 103 with polarity inverter 105, column 15, lines 49-50 indirectly receiving inversion signal line 112 via flipflop 107 in figure 6) for generating an inverting signal (output of inverting circuit 105 shown in figure 6), and outputting the inverting signal (signal input to switch 106b in figure 6). For rejection purpose, it is interpreted that the data signal corresponds to the output of the comparator 3 of figure lA that becomes high (column 10, lines 61-62), that the second power corresponds to that of waveshaper 4 of figure 1 B and this corresponds to the claimed "lifting the high state by as much as the second power". However, Akiyama et al. fails to expressly teach a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel. Note figure IA indicates each pixel comprises a comparator and waveform shaper 4, also note column 12, power of driver circuits can be turned

off, column 12, line 32, opposite electrode driving circuit 904 providing voltage Vcom shown in figure 9 and Vcom corresponds to the claimed third power. It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus Akiyama et al. then provide a power unit for supplying a first power and a second power in order to energize the comparator and wave shaper for driving the LCD with AC voltage in order to reduce power consumption.

As to claim 6, the liquid crystal display (LCD) of claim 5, further comprising a memory cell unit (memory 803, figure 8).

As to claim 7, the liquid crystal display of claim 6, wherein the memory cell unit receives the first and second control signals from the control signal line unit (note Vref and Vcs being received by block 15 as shown in figure IA/B) and receiving the inverting signal of the second control signal output by the level shift unit (column 15, lines 60-62).

As to claim 8, the liquid crystal display (LCD) of claim 7, wherein an operation mode image signal is selectively output to a third electrode of the pixel switch (scanning signal activates switching transistor 1 shown in figure 6, column 9, lines 57-59) and the operation mode signal is selectively transmitted to the liquid crystal unit (waveform shaper 4 output to the liquid crystal 5, as shown in figure 1 A).

As to claim 11, the liquid crystal display (LCD) of claim 5, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions (buffer circuit has to exist in LCD driving circuit shown in figure 9 in order to remove

noise, LCD panel 901 is divided into pixel arrays by signal lines 8 and gate lines 9, column 9, lines 47-54).

As to claim 12, Akiyama et al. discloses in a liquid crystal display (LCD) panel comprising a pixel switch (transistor 1 shown in figure 1 A) that receives scanning signals and image signals from scanning lines and source signal lines (column 9, lines 47-48) to output the image signals to a memory cell unit (memory 803 shown in figure 8), an LCD driving method comprising: the memory cell unit (memory 803 shown in figure 8) transmitting operation mode signals output by the pixel switch to liquid crystal and display the same (data signal for moving picture, column 18, lines 5-7) ; and transmitting either a still mode image signal (data signal is supplied to the pixel , column 9, lines 57-58, figure 9 indicates still picture as input signals) output by a third electrode of the pixel switch or its inverting signal (polarity inverter 105, column 15, lines 4950) to the liquid crystal (AC voltage applied to liquid crystal , column 3, lines 23-24 DC) as the second control signal periodically repeats low and high states (Very is AC voltage as shown in figures 11 C/D) to fit characteristics of an LCD panel . However, Akiyama et al. fails to expressly teach when the first control signal is in low state and the second control signal is in high state. One skilled in the art would know how to selectively control a memory cell in order to read/write. Note that Akiyama et al. teaches different image signals from still picture and moving picture (figure 9). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the method Akiyama et al. then provide selective control of the memory in order to accommodate driving the LCD with plurality of image signal types (still picture and moving picture).

As to claim 13, the method of claim 12, wherein the method further comprises transmitting respective control signals sequentially delayed by a buffer circuit to a corresponding pixel area where the pixel area of the LCD panel is divided into at least two portions in either a horizontal or vertical direction (buffer circuit has to exist in LCD driving circuit shown in figure 9 in order to remove noise, LCD panel 901 is divided into pixel arrays by signal lines 8 and gate lines 9, column 9, lines 47-54).

As to claim 14, the liquid crystal display of claim 7, wherein a still mode image signal (still picture from memory 908 of figure 9) is selectively output to the third electrode of the pixel switch (column 9, lines 57-59).

As to claim 15, the liquid crystal display of claim 7, wherein an inverting signal is selectively transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states (Akiyama et al. teaches Vref in form of alternating signal shown in figure 11 C, this implies still picture driving signal is periodically inverted) according to characteristics of the LCD panel.

Allowable Subject Matter

7. Claims 3 and 9-10 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

11/22/04

XIAO WU
PRIMARY EXAMINER